

EE 2381 DIGITAL COMPUTER LOGIC

Homework #12
19 Apr 2007

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Due: 26 Apr 2007

Review Text: Chapter 7, sections 1-3 and 5-8.

1. The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?
 - a. $8K \times 64$.
 - b. $4G \times 8$.
 - c. $256M \times 16$.
 - d. $8G \times 32$.
2. Give the number of bytes stored in the memories listed in Problem 1 above.
3. Word number 421_{10} in the memory shown in Mano Fig 7-3 contains the binary equivalent of $38,586_{10}$. List the 12-bit address and the 16-bit memory content of the word as a hexadecimal number.
4. Given a 64×8 ROM chip with an enable input, show the external connections necessary to construct a 512×8 ROM with eight 64×8 ROM chips and a decoder.
5. Tabulate a truth table for an 8×4 ROM that implements the following four Boolean functions:

$$A(X, Y, Z) = \sum m(1, 3, 5)$$

$$B(X, Y, Z) = \sum m(1, 3, 5, 7)$$

$$C(X, Y, Z) = \sum m(1, 3, 4, 5, 6, 7)$$

$$D(X, Y, Z) = \sum m(1, 5, 6, 7) .$$

6. Obtain the PLA programming table for the four Boolean functions listed in problem 5. Minimize the number of product terms. Be sure to attempt to share product terms between functions. You do not have to consider the usage of complemented outputs, but may chose to do so.
7. The following is a truth table of a 3-input, 4-output combinational circuit. Tabulate the PAL programming table for the circuit and mark the fuse map in a PAL diagram similar to the one shown in Fig. 7-17 in Mano on p. 284.

Inputs			Outputs			
x	y	z	A	B	C	D
0	0	0	0	1	1	1
0	0	1	0	1	0	0
0	1	0	1	1	0	1
0	1	1	1	1	1	1
1	0	0	1	0	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	1
1	1	1	1	0	1	1