

# EE 2381 DIGITAL COMPUTER LOGIC

Homework #9  
27 Mar 2007

Professor Jim Dunham  
Due: 05 Apr 2007

Review Text: Chapter 4, sections 5-7.

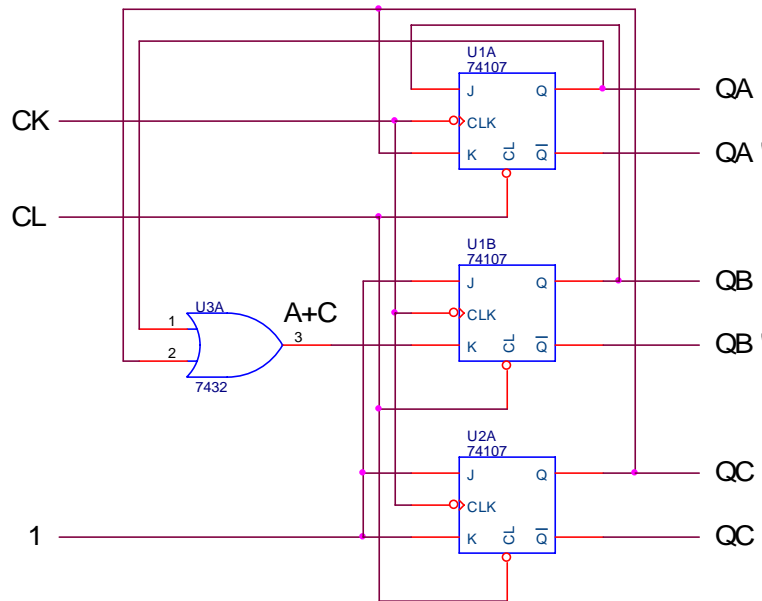
1. Draw a timing diagram for the circuit shown below using the following stimulus pattern:

The clock "CK" starts at time 0 with a value of 0, and then changes every 100 time units.

The clear "CL" starts as at time 0 with a value of 1. 50 time units later it goes to a 0. 200 time units later it returns to a 1 and then remains a 1 for the rest of the simulation.

The simulation continues for a total of six complete clock cycles (1200 time units).

Assume that the rise time and fall time delays for the J-K flip-flop outputs are 15 time units from appropriate changes on the clear and clock. Assume that the rise time delay of the OR gate is 20 time units and that the fall time delay is 15 time units.



2. Write a Verilog program which models the circuit shown below and stimulate it with the stimulus pattern used in problem 1. Assume that the rise time and fall time delays for the D flip-flop outputs are 14 ns and 20 ns, respectively, from appropriate changes on the clear and clock. Please use the Verilog submodule named `dff_7474` to implement the 7474 flip-flops (you do not need to develop these models). Assume that the rise time and fall times for the AND and OR gates are those used in EE 2181 lab #05 “Combinational Logic Design” for the 7400 TTL Logic Family. Please provide a copy of your Verilog program and a graphical timing diagram showing CK, CL, QA, QB and QC.

