EE 2381 DIGITAL COMPUTER LOGIC

Homework #7 **Professor Jim Dunham**
06 Mar 2007 **Due: 20 Mar 2007**

Review Text: Chapter 1, section 5-8 and Chapter 4, sections 4-7.

1. Find the truth-table for the first stage of a parallel adder shown in Fig P4-17 on p. 163 in Mano using Verilog simulation. You may wish to set all gate delays to zero so that it will be easier to interpret your simulation results. Be sure to include a copy of your Verilog code as well as the simulation output. Code the circuit exactly as shown in Mano Fig P4-17. Is this a full-adder?

2. Obtain the 1's and 2's complements of the following binary numbers:
   a. 11101110
   b. 01001101
   c. 00001000
   d. 10000000
   e. 00000000.

3. Perform subtraction on the following unsigned binary numbers using all three subtraction methods discussed in class.
   a. 11001 – 10101
   b. 1001 – 110110
   c. 100111 – 110000.

4. Perform the indicated arithmetic operation on the following 8-bit binary numbers assuming that they represent signed magnitude numbers. Verify your answer.
   a) $10110100_2 - 00101000_2$.
   b) $11001011_2 + 10111100_2$.
   c) $01110011_2 + 10100011_2$.
   d) $01110000_2 - 10010100_2$.

5. Repeat problem 4 assuming that the 8-bit numbers represent 2's complements numbers.

6. The adder-subtractor circuit of Mano Fig 4-13 has the following values for the mode input *M* and data inputs *A* and *B*. In each case, determine the values of the four SUM outputs, the carry *C*, and overflow *V*.

	M	A	B
(a)	0	0100	0110
(b)	0	0101	1011
(c)	1	1011	1010
(d)	1	0010	0110

7. Design a combinational circuit that adds 48_{10} to an 8-bit 2's complement binary number. Consider using half-adders and full-adders in your design. Be sure to indicate if an overflow has occurred. Finally, minimize the hardware needed to implement your design.

8. Simplify the following Boolean function

   $$F(W, X, Y, Z) = \sum m(0, 4, 5, 11)$$

   together with the don't care conditions

   $$d(W, X, Y, Z) = \sum m(2, 8, 9, 12, 13, 14, 15)$$

   into a minimal sum-of-products.