

EE 2381 DIGITAL COMPUTER LOGIC

Homework #6
27 Feb 2007

Professor Jim Dunham
Due: 06 Mar 2007

Review Text: Chapter 4, sections 1-3, and 8-11 (skim three-state gate materials).

- Find the truth-table for the 4-input priority encoder shown in Fig 4-23 on p. 141 in Mano using Verilog simulation. You may wish to set all gate delays to zero so that it will be easier to interpret your simulation results. Be sure to include a copy of your Verilog code as well as the simulation output. Code the circuit exactly as shown in Mano Fig 4-23.

- Construct a 4-to-16-line decoder with five 2-to-4-line decoders (74LS139A). Use a block diagram for components and clearly show your address select variables.

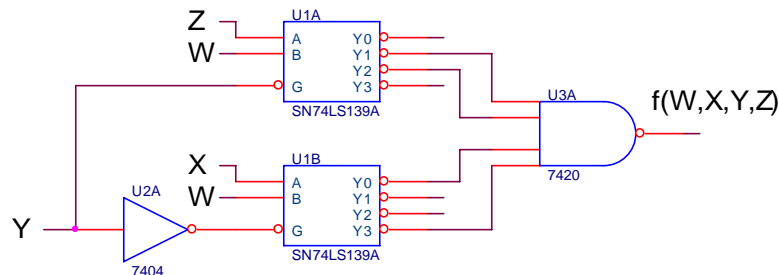
- Mano 4-27. Use the following functions:

$$F_1(A, B, C) = \sum m(1, 5, 6)$$

$$F_2(A, B, C) = \sum m(4, 6)$$

$$F_3(A, B, C) = \sum m(2, 3, 6, 7).$$

- For the hierarchical circuit below, find the truth-table for the output $f(W, X, Y, Z)$. Note that each decoder is a 74LS139A dual 2-line to 4-line decoder/demultiplexer.



- Construct a 32×1 multiplexer with four 8×1 (74LS151) and one 4×1 (74LS153) multiplexers. Use block diagrams and clearly show your address select variables.

- Mano 4-35. Use the following function:

$$F(A, B, C, D) = \sum m(0, 4, 7, 9, 10, 12, 15).$$