

EE 2381 DIGITAL COMPUTER LOGIC

Homework #4
06 Feb 2007

Professor Jim Dunham
Due: 13 Feb 2007

Review Text: Chapter 3, section 6-8 and Chapter 10, sections 1 and 2.

- Convert the following expression into product-of-sums (POS) form:

$$(AC + D)(\overline{A}B + \overline{A}\overline{B}\overline{C} + D).$$

- Simplify the following function into minimal product-of-sums (POS) form:

$$F(W, X, Y, Z) = \prod M(0,1,2,4,5,6,8,9,10).$$

- Simplify the following Boolean function F

$$F(W, X, Y, Z) = \sum m(1,11,15)$$

together with the don't care conditions

$$d(W, X, Y, Z) = \sum m(0,6,7,9,14)$$

into minimal product-of-sums (POS) forms.

- Simplify the following expression and implement it with a two-level NAND gate circuit:

$$\overline{A}C + \overline{A}BC + \overline{A}C\overline{D} + B\overline{C}D.$$

- Draw a logic diagram using only two-input NAND gates to implement the Boolean expression in problem 4. How does this differ from the realization in problem 4?

- Implement the Boolean function in problem 4 with a two-level NOR gate circuit.

- Draw a logic diagram using only two-input NOR gates to implement the Boolean expression in problem 4. How does this differ from the realization in problem 6?

- Implement the Boolean function F in problem 4 using the two-level forms (a) NAND-AND, (b) AND-NOR, (c) OR-NAND, and (d) NOR-OR.

- Find t_{pHL} , t_{pLH} and t_{pd} for a CD4001BC Quad 2-Input NOR Gate when V_{DD} is 5V, 10V and 15V.

- Assuming that each gate in figure below has an average propagation delay $t_{pd} = 17.5$ ns, what is the propagation delay of the longest path through the circuit?

